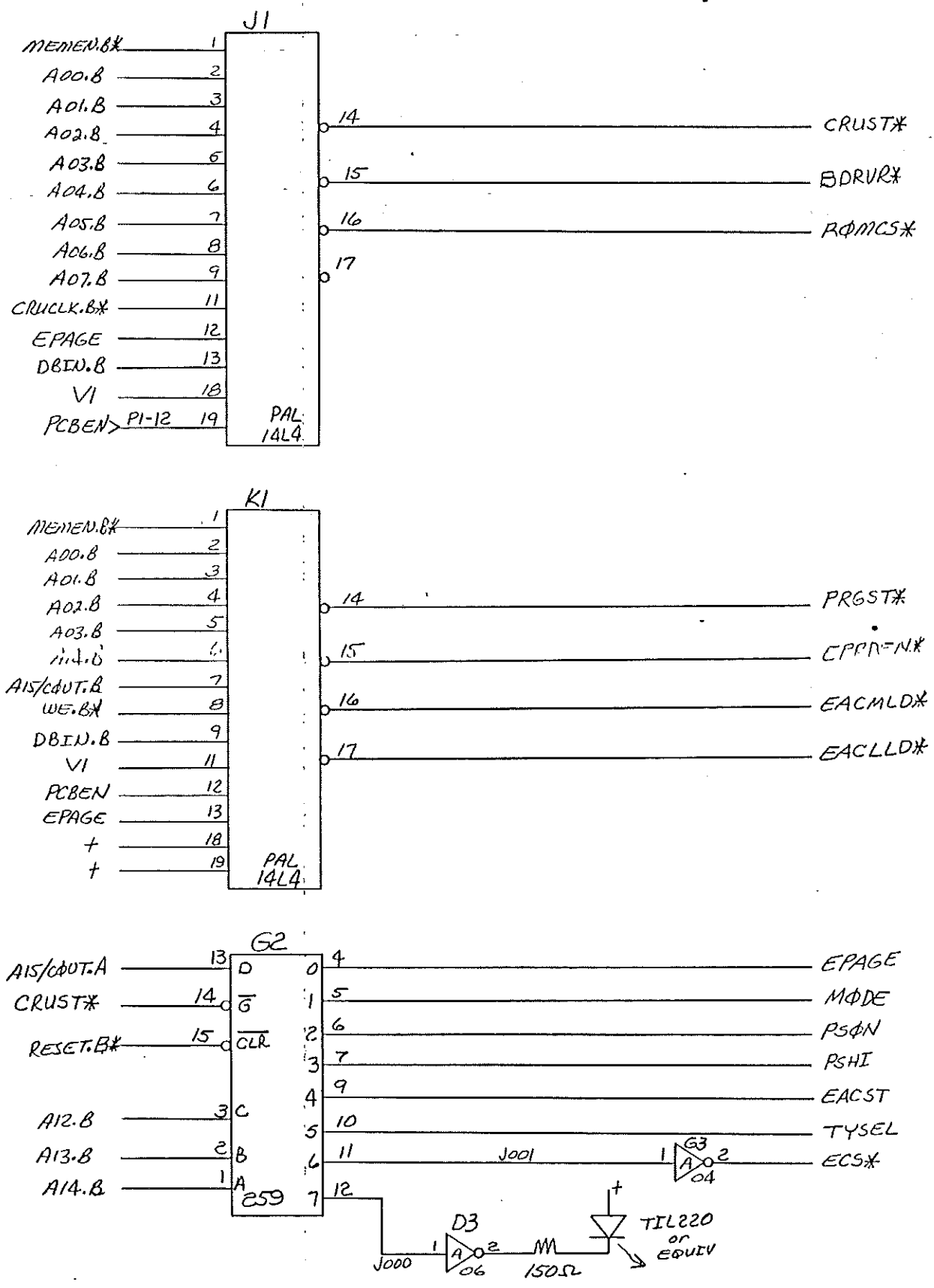
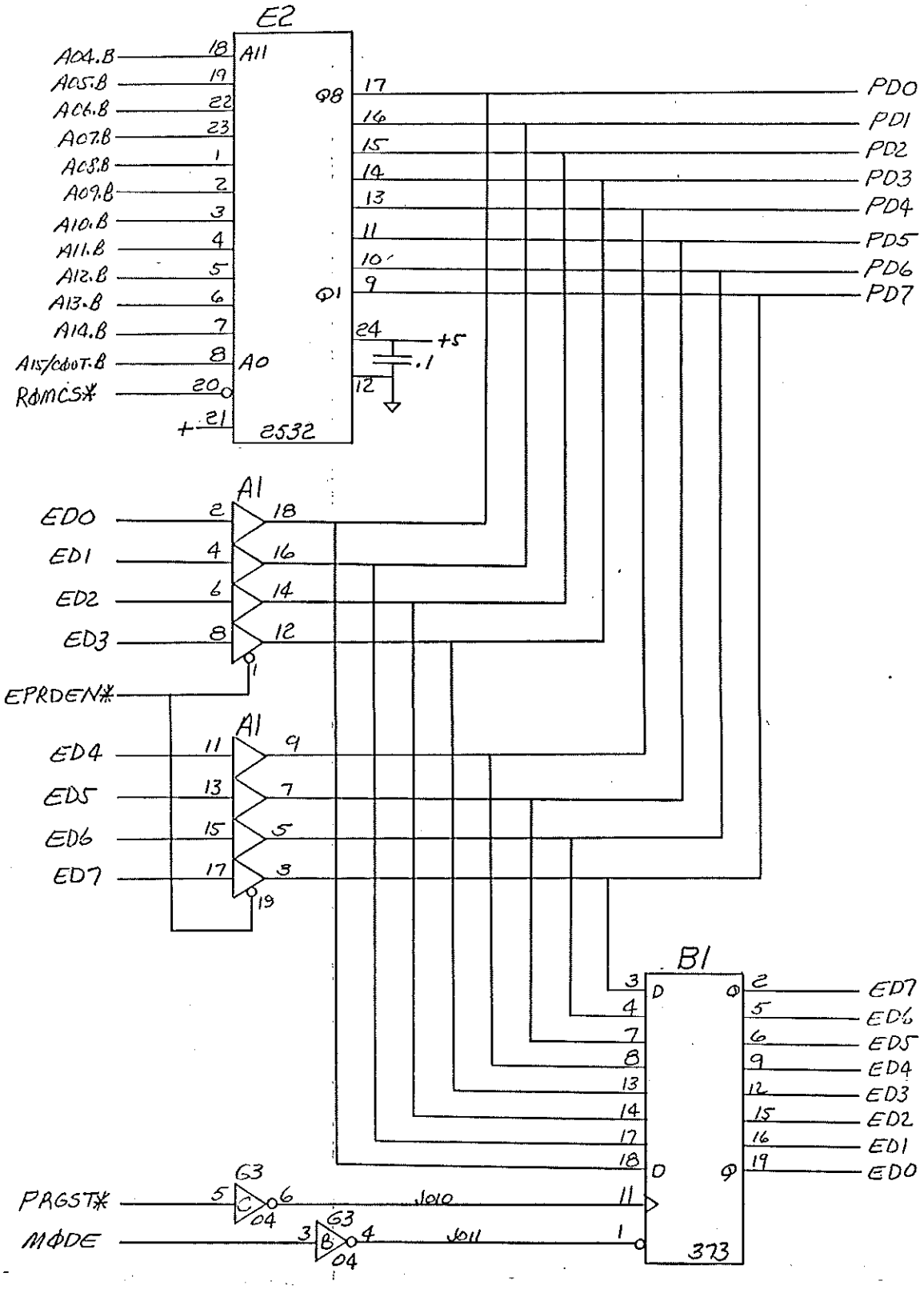


PLAs, CRUØUT REG

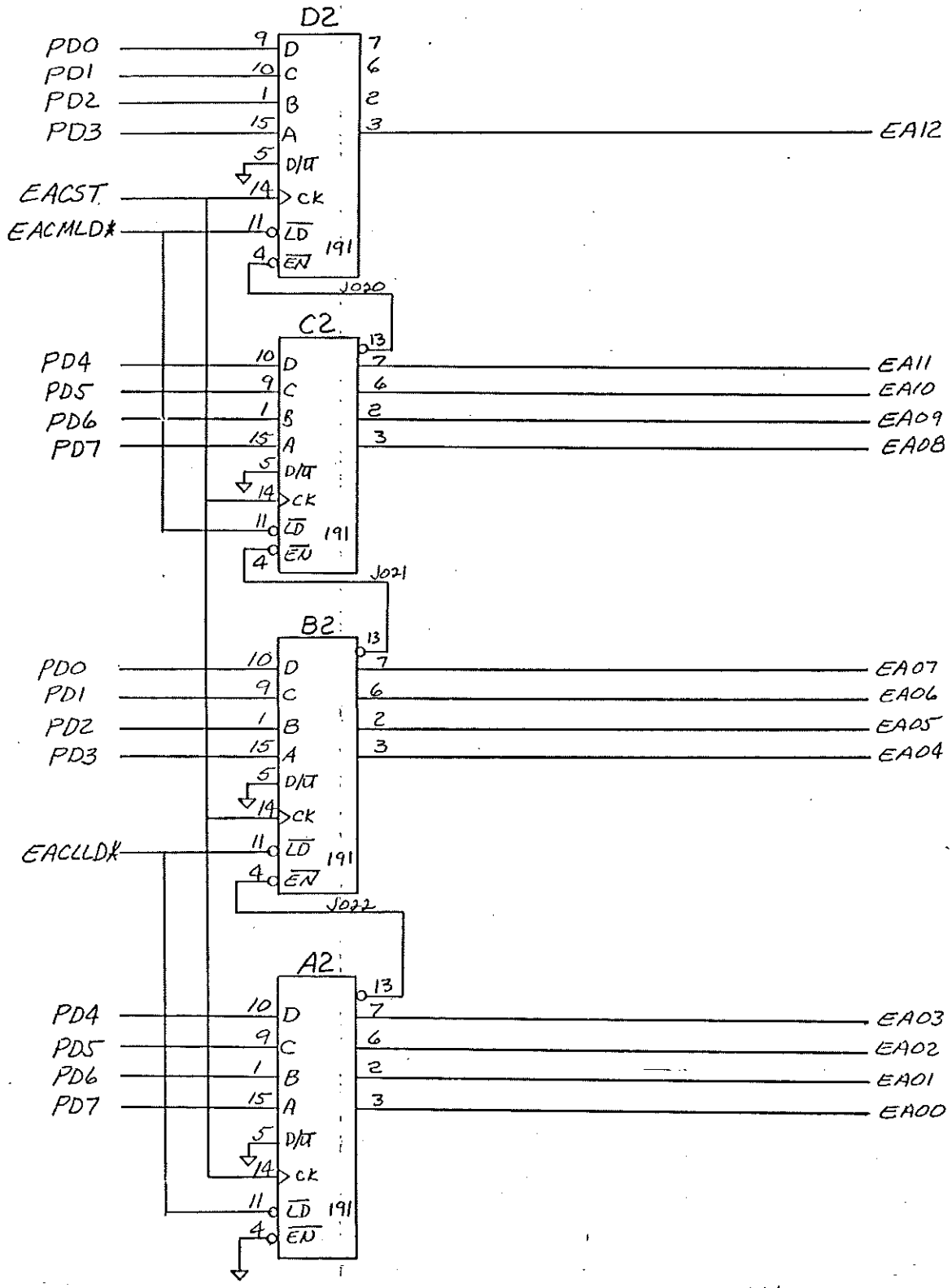
3/31/82
3/30/82



(2)

3/30/82
TILFB

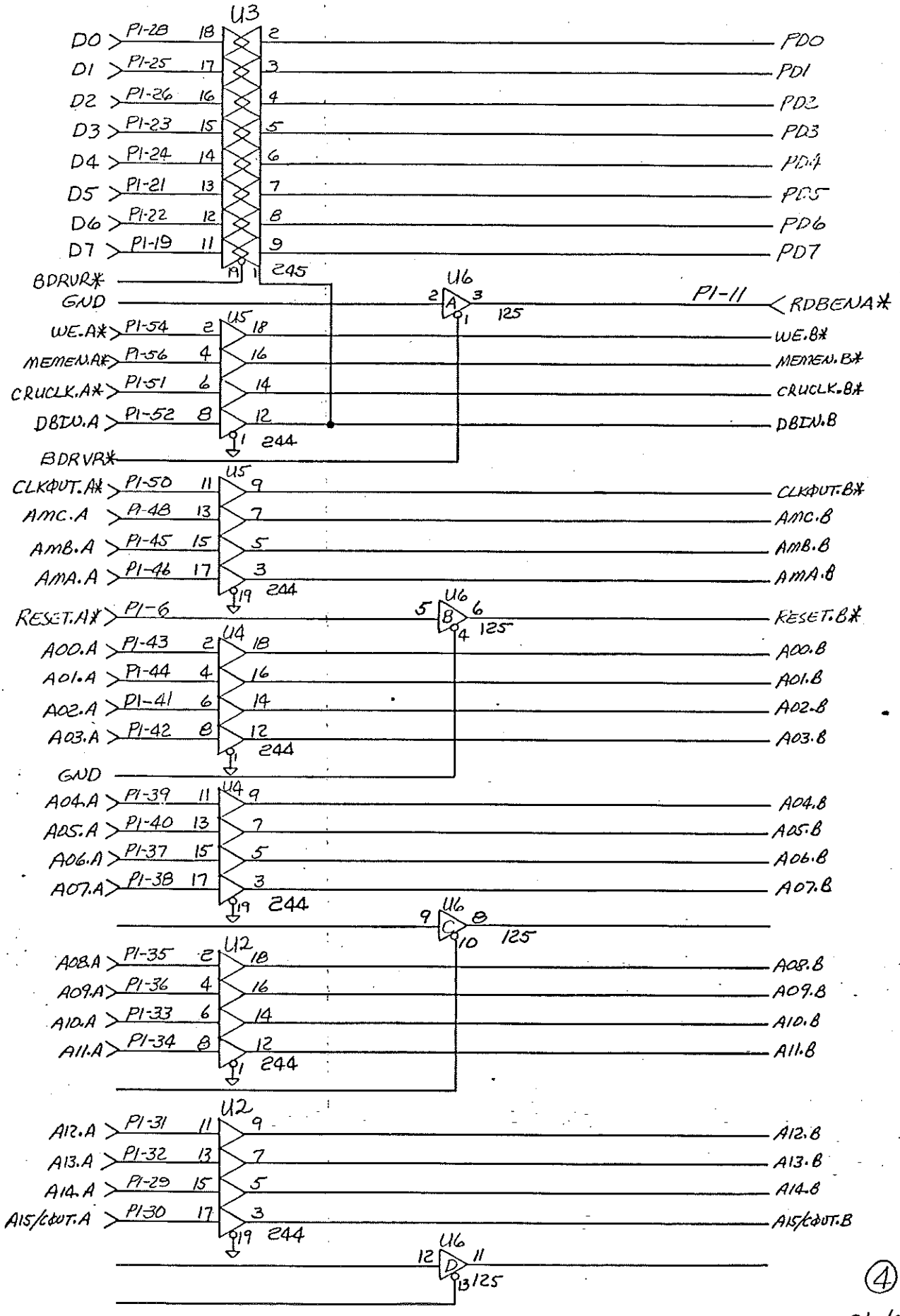
DSR ROM, EPROM READ/WRITE BUS



EPROM ADDRESS COUNTERS

3

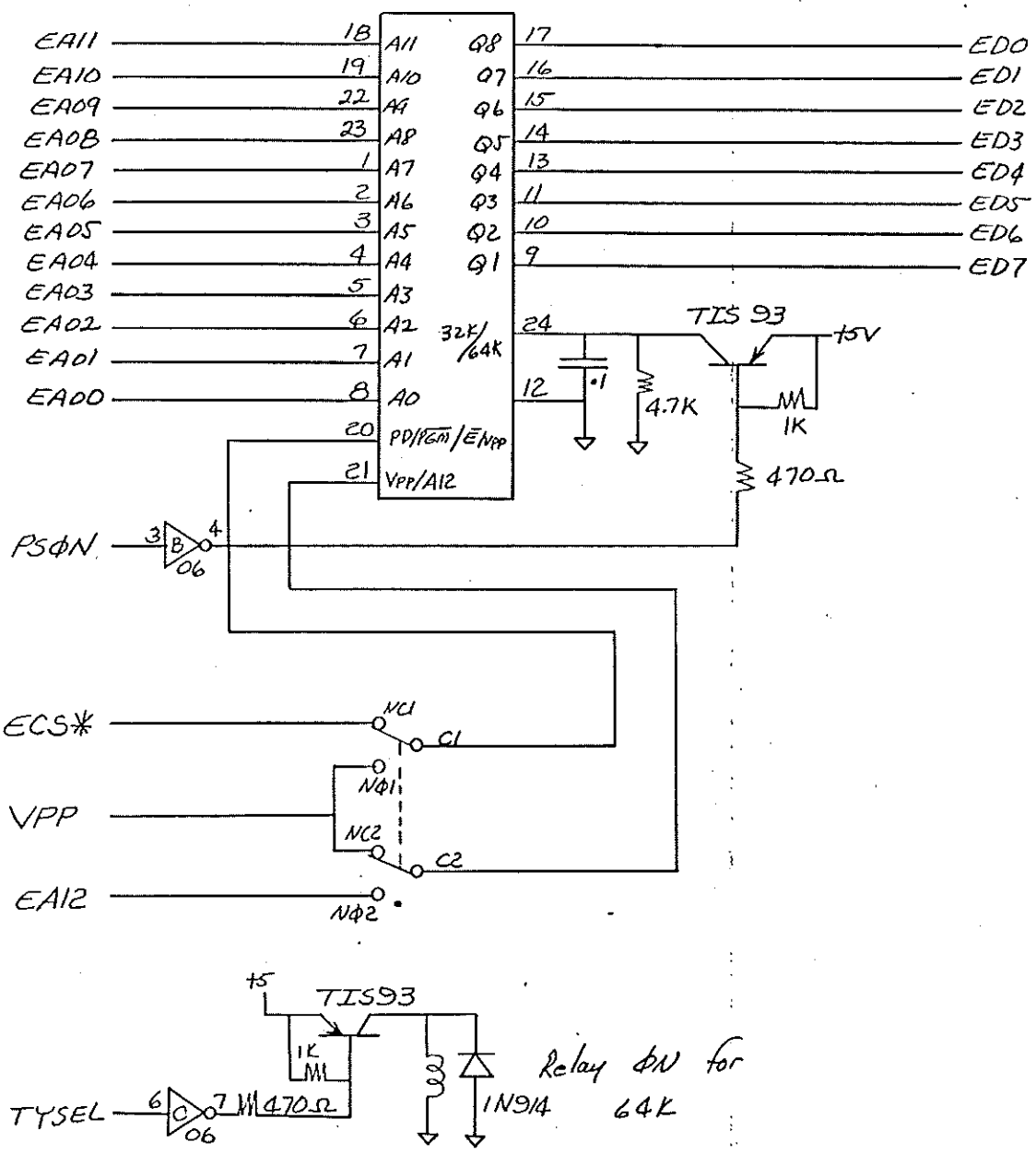
5/31/82



4

3/30/82 mh

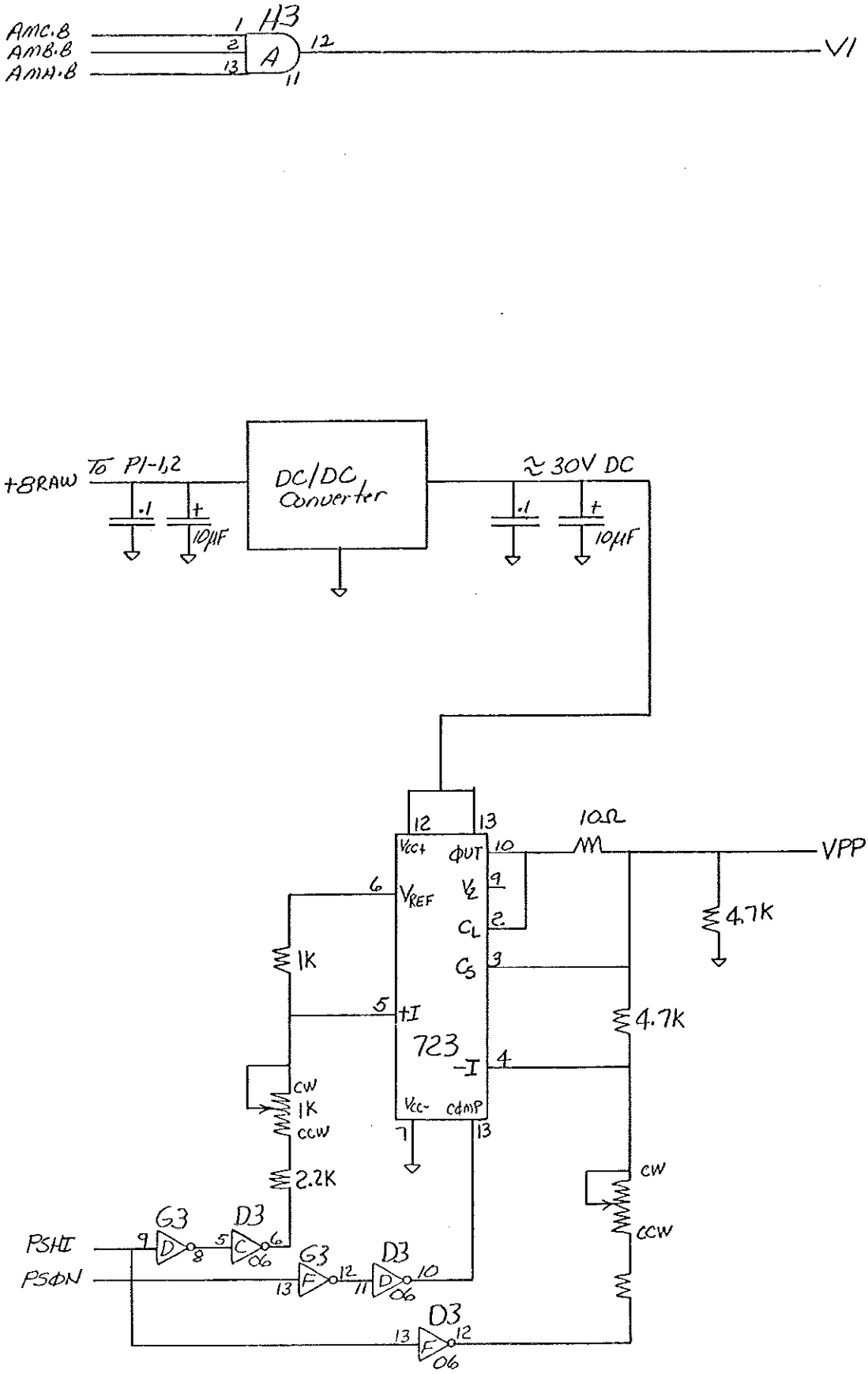
SYSTEM BUS INTERFACE



(5)

3/31/82

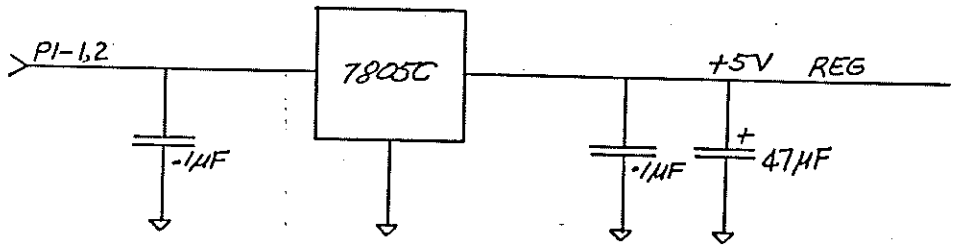
MMP Control Logic



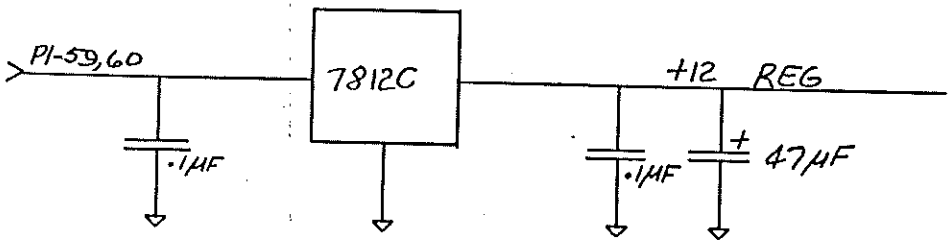
(6)

4/29/82
3/31/82
MTB

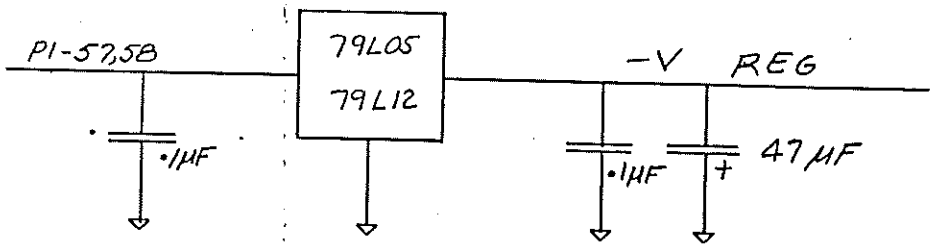
Misc Logic



NOT USED



NOT USED.



3/30/82
mfb

3T REGs

# CRU Bit Definition
Base = >1000

Disp	Function
0	DSR ROM Page bit
1	MODE 0 = READ, 1 = PROGRAM
2	Power supply enable, 0 = OFF, 1 = ON, LEDals.
3	Power supply Voltage Control, 0 = +5V, 1 = +25
4	Address CTR Increment SBO/SBZ
5	2532/2564 select 0 = 2532, 1 = 2564
6	EPROM $\overline{CE}$ 0 = $\overline{CE}$ = 1, 1 = $\overline{CE}$ = 0
7	Verify LED 0 = OFF, 1 = ON

PAL #1

16L4

1	/MEMEN	11	/CRUCLK
2	A0	12	EPAGE
3	A1	13	DBIN
4	A2	14	/CRUST
5	A3	15	/BDRVR
6	A4	16	/ROMCS
7	A5	17	open output
8	A6	18	VI
9	A7	19	PCBEN
10	Power GND	20	VCC

/CRUST = /MEMEN * /A0 * /A1 * /A2 * A3 * /A4 * /A5 * /A6 * /A7 * CRUCLK * PCBEN

/BDRVR = MEMEN * /A0 * A1 * /A2 * EPAGE * PCBEN * VI

/ROMCS = EPAGE * MEMEN * /A0 * A1 * /A2 * /A3 * DBIN * VI * PCBEN

3/30/82
WB

PLA #2 PAL19L4

1	/MEMEN	11	VI
2	A0	12	PCBEN
3	A1	13	EPAGE
4	A2	14	/PRGST
5	A3	15	/EPRDEN
6	A14	16	/EA CMLD
7	A15COUT	17	/EA CLLD
8	/WE	18	GND
9	DBIN	19	GND
10	Power GND	20	VCC

PRGST = VI*MEMEN*WE*/A0*A1*/A2*A3*/A14*PCBEN
*/A15COUT*EPAGE

EPRDEN = VI*MEMEN*DBIN*/A0*A1*/A2*A3*/A14*
EPAGE*PCBEN*/A15COUT

EACMLD = VI*MEMEN*WE*/A0*A1*/A2*A3*A14*/A15COUT
*EPAGE*PCBEN

EACLLD = VI*MEMEN*WE*/A0*A1*/A2*A3*A14*A15COUT
EPAGE*PCBEN

3/30/82

# CRU Bit Definition
Base = >1000

Disp	Function
0	DSR RØM Page bit
1	EPRØM Mode 1 = Program, 0 = READ
2	Power supply enable, 0 = ØFF, 1 = ØN, LED ctl
3	Power supply Voltage Control, 0 = +5V, 1 = +25
4	Address CTR Increment 5BØ/5BE ⊓⌐
5	2532/2564 select 0 = 2532, 1 = 2564
6	EPRØM $\overline{CE}$ 0 ≡ $\overline{CE}$ = 1, 1 ≡ $\overline{CE}$ = 0
7	Verify LED 0 = ØFF, 1 = ØN

Memory Space

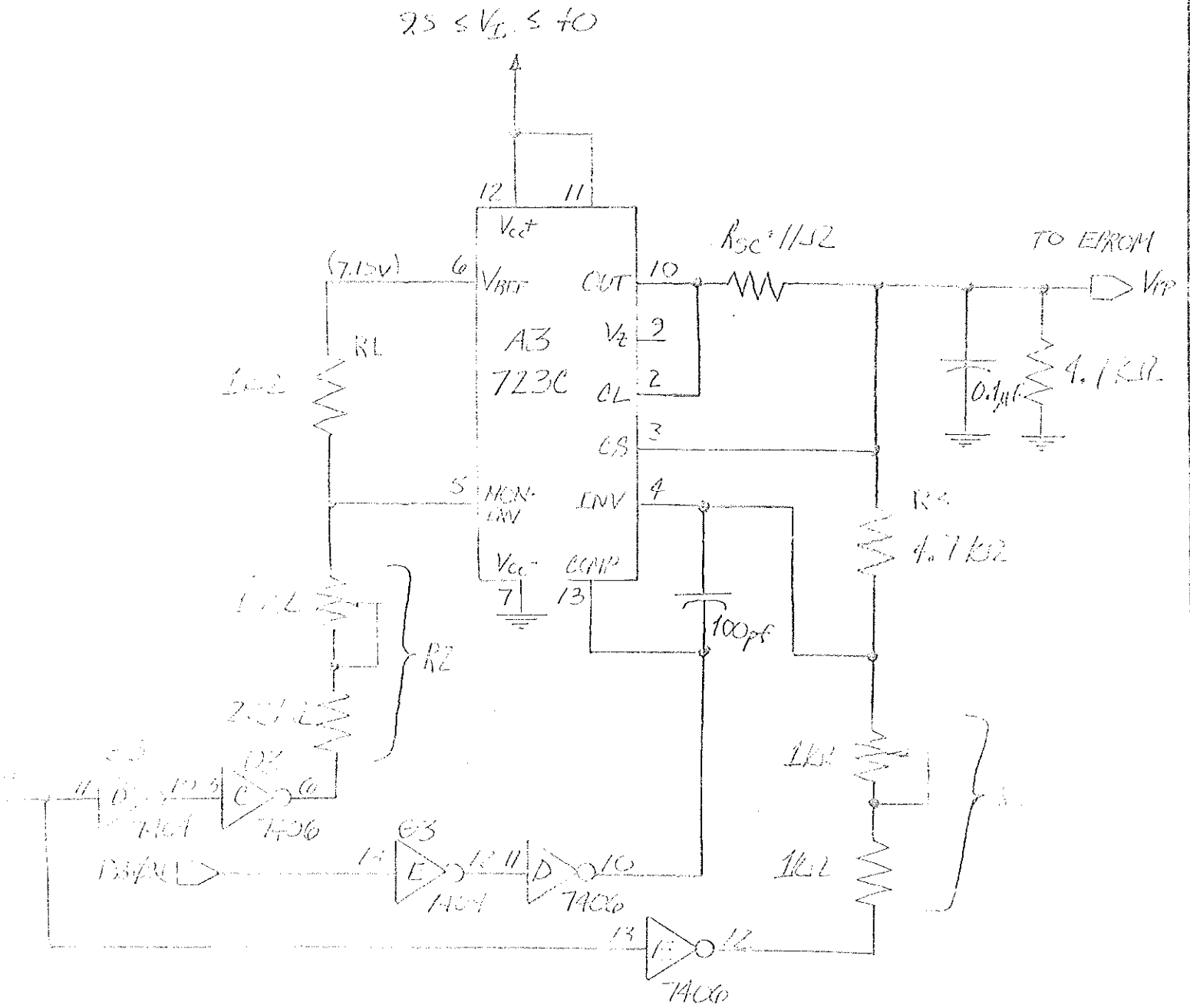
>4000 - >4FFF DSR ROM

>5000 EPROM READ, EPROM Write Register

>5002, 3 EPROM ADDRESS CTR LOAD

3/30/82
MB

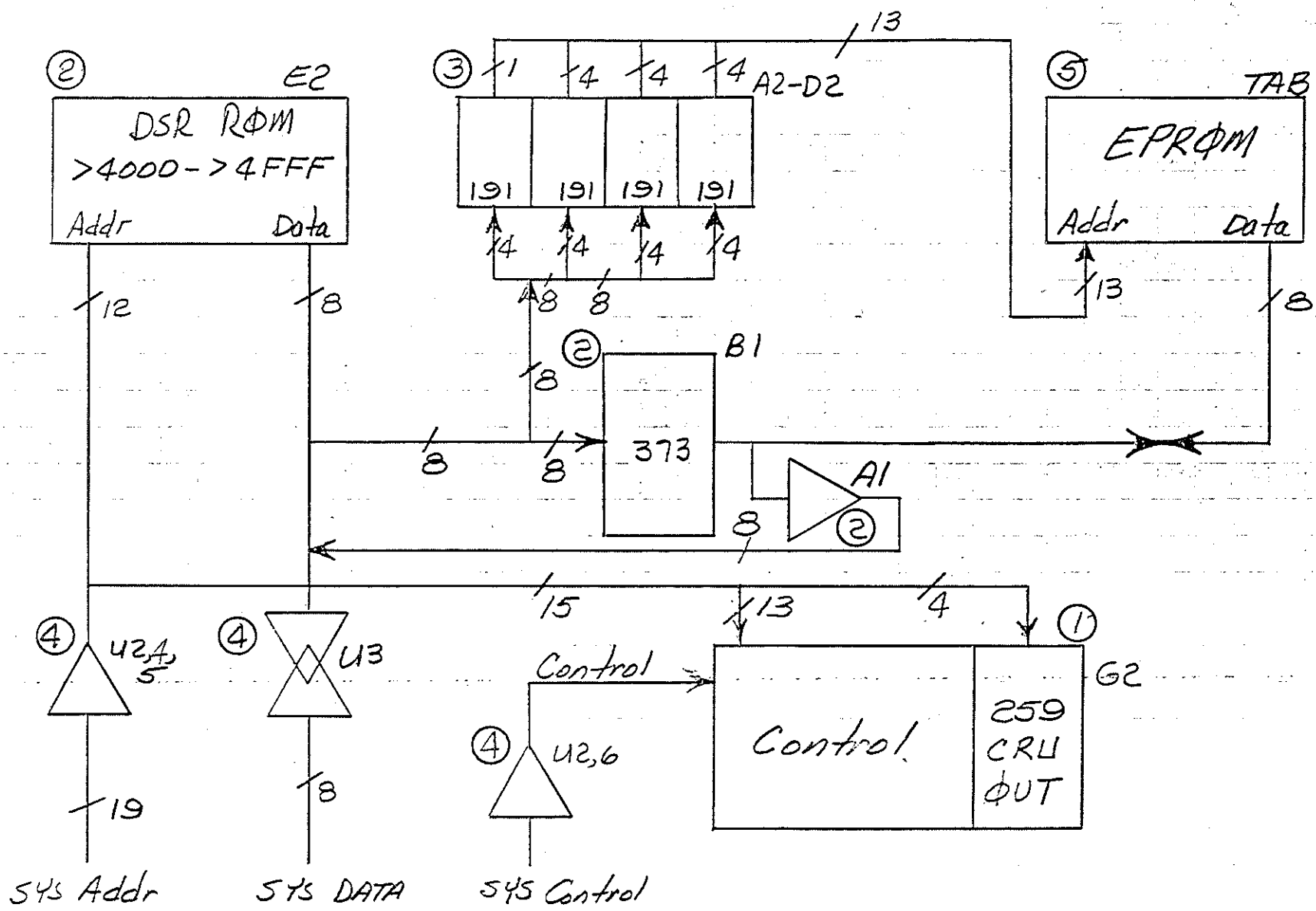
μA723C



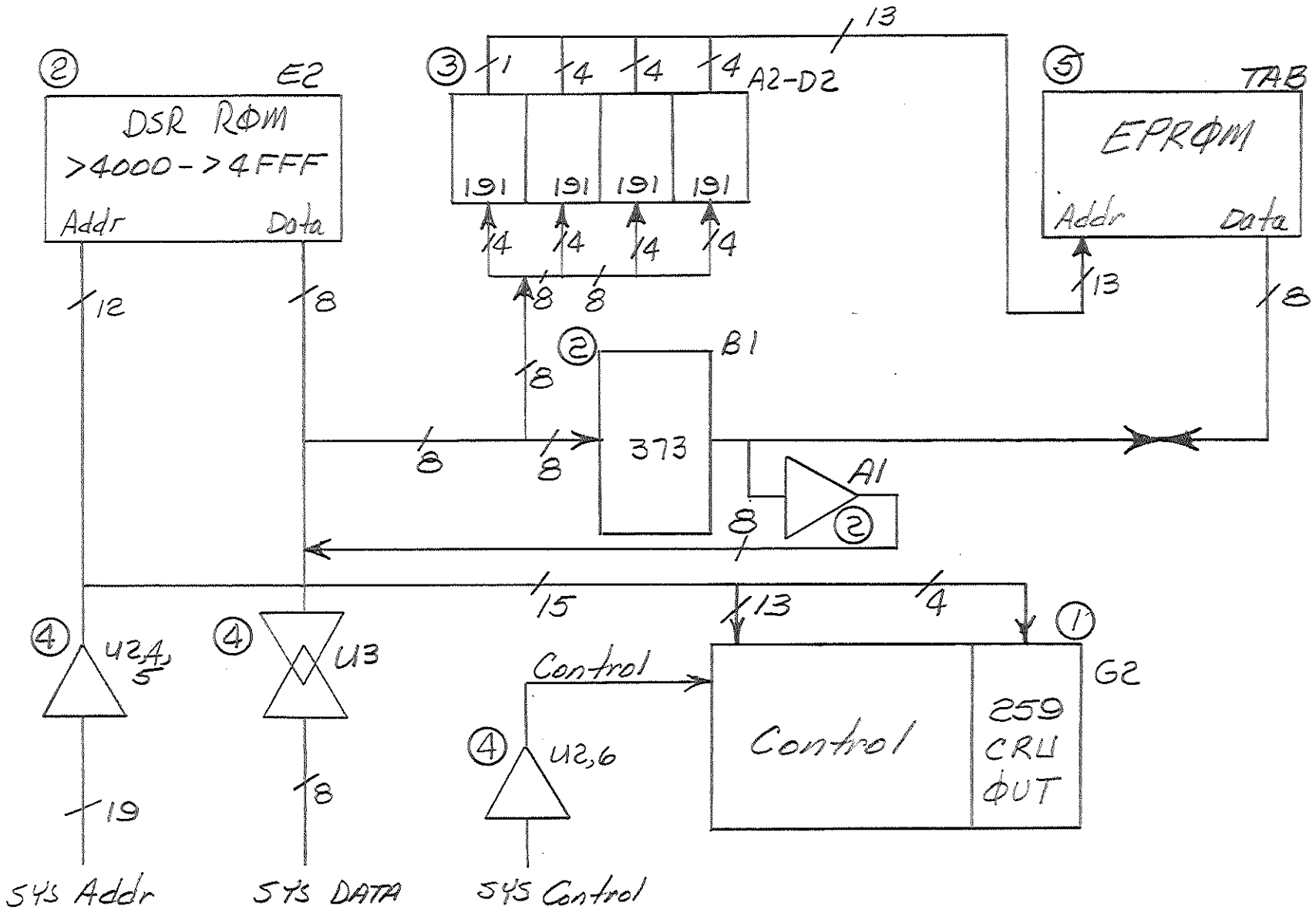
TYPICAL ADJUSTMENT RANGES OF OUTPUT: POS'E = Ø : (4.5 ≤ V_PP ≤ 5.1)
POS'E = 1 : (13.5 ≤ V_PP ≤ 45.1)

CLMP
9/2/82

CONDUCTOR SIDE
1039332


2
E2
DSR ROM
>4000->4FFF
Addr
Data
3
1
4
4
4
A2-D2
191
191
191
191
13
5
TAB
EPROM
Addr
Data
12
8
8
8
8
2
B1
373
A1
2
8
8
8
8
15
13
4
4
U2,4,5
4
U3
4
U2,6
Control
Control
259
CRU
OUT
G2
1
19
8
SYS Addr
SYS DATA
SYS Control

3/30/82
MFB


2
E2
DSR ROM
>4000->4FFF
Addr
Data
12
8
3
1
4
4
4
A2-D2
13
191
191
191
191
4
4
4
4
8
8
5
TAB
EPROM
Addr
Data
13
8
2
B1
8
373
8
8
A1
2
8
15
13
4
1
G2
4
U2,4,5
4
U3
Control
4
U2,6
Control
259
CRU
OUT
19
8
SYS Addr
SYS DATA
SYS Control

3/30/82
MFB